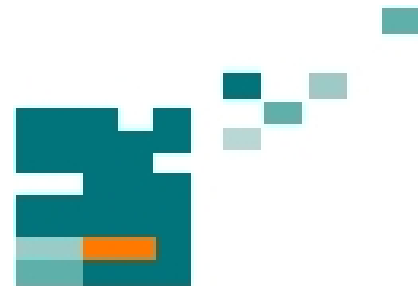


54. IWK

Internationales Wissenschaftliches Kolloquium
International Scientific Colloquium



Information Technology and Electrical Engineering - Devices and Systems, Materials and Technologies for the Future



Faculty of Electrical Engineering and
Information Technology

Startseite / Index:

<http://www.db-thueringen.de/servlets/DocumentServlet?id=14089>

Impressum

Herausgeber: Der Rektor der Technischen Universität Ilmenau
Univ.-Prof. Dr. rer. nat. habil. Dr. h. c. Prof. h. c.
Peter Scharff

Redaktion: Referat Marketing
Andrea Schneider

Fakultät für Elektrotechnik und Informationstechnik
Univ.-Prof. Dr.-Ing. Frank Berger

Redaktionsschluss: 17. August 2009

Technische Realisierung (USB-Flash-Ausgabe):
Institut für Medientechnik an der TU Ilmenau
Dipl.-Ing. Christian Weigel
Dipl.-Ing. Helge Drumm

Technische Realisierung (Online-Ausgabe):
Universitätsbibliothek Ilmenau
[ilmedia](#)
Postfach 10 05 65
98684 Ilmenau

Verlag:  Verlag ISLE, Betriebsstätte des ISLE e.V.
Werner-von-Siemens-Str. 16
98693 Ilmenau

© Technische Universität Ilmenau (Thür.) 2009

Diese Publikationen und alle in ihr enthaltenen Beiträge und Abbildungen sind urheberrechtlich geschützt.

ISBN (USB-Flash-Ausgabe): 978-3-938843-45-1
ISBN (Druckausgabe der Kurzfassungen): 978-3-938843-44-4

Startseite / Index:
<http://www.db-thueringen.de/servlets/DocumentServlet?id=14089>

EQUIVALENT SCHEME OF THE DEVICE WITH THE CHARGE LINK GUIDED BY THE P-N-JUNCTION

Nikolai Tsyrelchuk, Elena Ruchaevskaia

INTRODUCTION

For the modeling the schemes with the metal dielectric semiconductor (MDS) devices with the charge link (DCL) usually the structure, consisting of a number of MDS-elements, separated by the gates, is considered. By analogy with this the devices with the charge link, guided by p-n junctions (DCLGJ), can be considered as a number of p-n-p (or n-p-n) vertical elements, separated by the gates. That's why for modeling the schemes on DCLGJ the model DCL itself and the gap model can be used.

MICRO- AND NANOELECTRONICS

We propose the simple electric DCLGJ model, where the interpretation of the transfer equations in the semiconductor with the help of the circuit equation was taken as a principle [1]. The structure fragment and the equivalent scheme of one element of DCLGJ are depicted in (see Fig. 1). Where 1 – gate region; 2 – channel region; 3 – base

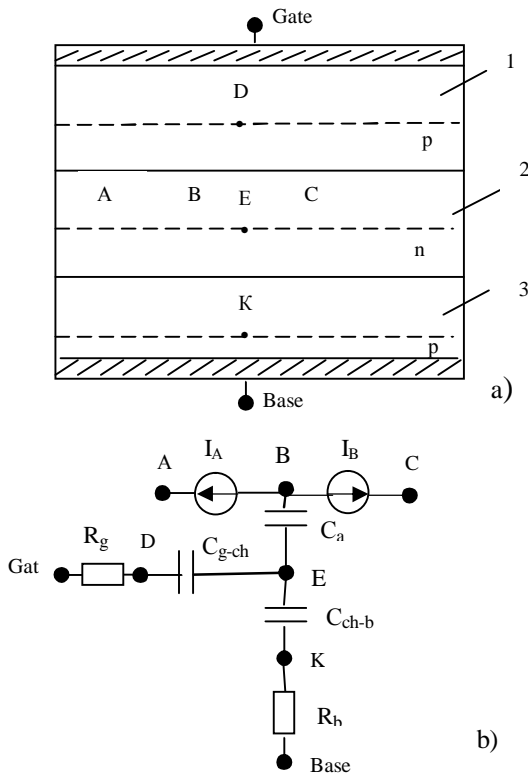


Figure 1 The structure fragment a) and equivalent scheme b) DCLGL element

On the equivalent scheme (Fig.1) C_{g-ch} и C_{ch-b} capacities correspond the capacities of the backward biased p-n junctions gate-channel and channel-base, accordingly. C_a – accumulation (storage) capacity of the electrons. R_b и R_g – ohmic resistances of the base and gate, accordingly, I_A и I_B – the current sources, taking into account the channel conductivity [1].

The points и A, B, C are three different points in the DCL channel, the voltage in which equals the value of the electron potential of the Fermi quasilevel F_p . The points D, K define the boundaries of the depleted layers in the gate regions and the base, accordingly. The voltage in the point E equals electrostatistical potential F_{ch} in this point, i.e. the potential channel. Capacities C_{g-ch} и C_{ch-b} are calculated by the formulae for the reverse drifted p-n junctions considering them to be a step-like.

The charge in the channel is accumulated on the condenser C_a . This condenser is charged and discharged by the I_A and I_B currents. Other possible mechanisms of charging and discharging of the C_a capacity, such as the thermal generation in the depleted layer, leakage. The value C_a capacity is calculated according to the expression:

$$C_a = \left(\frac{e_o e_n q n_i}{2j_T} \right)^{\frac{1}{2}} \exp \left(\frac{F_{ch} - F_p}{2j_T} \right)$$

The formulae for the current sources are resulted in the majority carriers and calculated by the following expressions:

$$I_A = 8m_n C_a \left(\frac{kT}{qL_g} \right)^2 \left[\exp \left(\frac{qV_{AB}}{2kT} \right) - 1 \right];$$

$$I_B = 8m_n C_a \left(\frac{kT}{qL_g} \right)^2 \left[\exp \left(\frac{qV_{BC}}{2kT} \right) - 1 \right]$$

Where L_g – the gate length; V_{AB} , V_{BC} – potential differences between the points AB и BC.

The given electrical model DCLGJ can be used for modeling DCL elements circuits, analysis on the transition process in the devices on the DCLGJ and for other purposes [1].

REFERENCES

- [1] N.Tsyrelchuk, I.Rusak., The devices with the Charge Connection Conducted by p-n transition. Foreign Electronic Technique, N 9, pp. 3 – 36, 2007.

[2] Tsyrelchuk N. Analogue-digital and digital-analogue transformers on the devices with the charge link, conducted by p-n transitions. – In book.: Perspectives of the development and application of the automated radiomeasuring apparatus in the national economy: theses of the report NTC, Minsk, – pp 7-10 , 2007.

[3] Kuznetsov J., Shilin V., Microschemotechnics on the devices with the charge connection. – M.: Radio and Communication, 160 p, 1998.